



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/109,261	06/30/1998	GANG BAI	042390.P5769	3347

7590 02/10/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025

EXAMINER

WARREN, MATTHEW E

ART UNIT	PAPER NUMBER
----------	--------------

2815

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/109,261
Filing Date: June 30, 1998
Appellant(s): BAI, GANG

MAILED

FEB 1 2006

GROUP 2800

William Thomas Babbitt
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 4, 2005 appealing from the Office action mailed January 26, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,015,281	Nagata et al.	3-1977
5,990,516	Momose et al.	11-1999
5,621,681	Moon	4-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8-10, 13-17, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al. (US 4,015,281) in view of Momose et al. (US 5,990,516) and Moon (US 5,621,681).

Nagata discloses (col. 3, line 45 – col. 4, line 67) a transistor device (figs. 21-25) having a gate electrode (96) overlying a gate dielectric (82 and 84) formed directly on a semiconductor substrate. The dielectric (col. 4, lines 34-49) comprises a first dielectric

having a first dielectric constant and a second dielectric having a second dielectric constant different from the first dielectric constant. The first and second dielectrics are scalable for a set of feature size technologies, wherein the first and second dielectric thickness are determined by the formula as recited in claims 8 and 15 (see the expanded formula in col. 4, lines 39-44). The second dielectric (Al_2O_3) has a greater dielectric constant than the first dielectric (SiO_2) (col. 4, lines 45-49). A third dielectric ($\text{SiO}_2\text{-P}_2\text{O}_5$), having a third dielectric constant may also be used in the composite dielectric layer (col. 4, lines 50-56). Nagata et al. shows all of the elements of the claims except the set of feature size technologies defined by a gate length in the range of 25-150 nm. Momose et al. discloses (col. 16, 28-48 and col. 16, line 66-col. 17, line 32) a semiconductor device having a double layer gate dielectric in which the feature size technology has a gate length of 150 nm (or 0.15 μm) to form a high performance semiconductor having low power consumption. Momose et al. further discloses (col. 15, lines 13-31) that the gate length can be decreased even more to improve the current drive capability. The gate in one embodiment had a length of 40 nm (0.04 μm). Momose et al. also discloses (col. 2, lines 52-58) a semiconductor device in which the thickness of the gate dielectric is less than 1/3 the gate length. The thin gate dielectric improves hot carrier reliability and ultimately the operating characteristics.

Nagata and Momose shows all of the elements of the claims except the first dielectric selected from the group of HfO_2 , BaO , La_2O_3 , Y_2O_3 and ZrO_2 . Moon shows a (fig. 2) a semiconductor device comprising a first dielectric material (11a) of Y_2O_3 and a second dielectric material (12a) of PZT which has a second dielectric constant greater

than the dielectric constant of the first dielectric. With this configuration, the yttrium oxide is used as a buffer dielectric and a good quality ferroelectric is formed on the substrate (col. 4, lines 1-12). Moon also shows that the transistor device is isolated from other devices by shallow trench isolation (2).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the multi-layer gate dielectric of Nagata for a feature size technology with a desired gate length as taught by Momose to form a high performance transistor having low power consumption. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the multi layer gate dielectric of Nagata and Momose by using Y_2O_3 and PZT as the first and second dielectric layer as taught by Moon to form a good quality ferroelectric on a substrate.

(10) Response to Argument

The appellant primarily argues that the cited references do not show all of the elements of the claims. The appellant specifically argues (1) that Nagata does not properly show "first and second dielectric materials being scalable for a set of feature size technologies, the set of feature size technologies defined by a gate length in the range of 25-70 nm, wherein the first material thickness (t_1) and the second material thickness (t_2) are determined by the relationship $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$ (eq. 4 cited in appellant's brief and cited in claims 8 and 15). The appellant also specifically argues (2) that Momose and Moon do not cure the deficiencies of Nagata by showing a gate length

Since the appellant does not use silicon dioxide or any other additional dielectrics in their two layered gate dielectric, $T_{SiO_2} = 0$, and the formula becomes:

$$\frac{T_{eff}}{E_{SiO_2}} = \left(\frac{D}{E_{SiO_2}} + \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \dots \frac{D}{E_{x1}} + \dots \frac{D}{E_{x_n}} \right)$$

and finally:

$$\frac{T_{eff}}{E_{SiO_2}} = \left(\frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \right)$$

When the variables of Nagata's equation are substituted with the variables of the appellant's equation,

$$\begin{aligned} T_{eff} &= t_{ox} & E_{SiO_2} &= k_{ox} \\ T_{x1} &= t_1 & T_{x2} &= t_2 \\ E_{x1} &= k_1, & E_{x2} &= k_2 \end{aligned}$$

Nagata's formula looks like:

$$\frac{t_{ox}}{k_{ox}} = \frac{t_1}{k_1} + \frac{t_2}{k_2}$$

Thus the equations of Nagata and the appellant are the same. Nagata's equation is more complete because it includes SiO_2 and as many additional layers as one desires to add to the multi-layered dielectric stack. Even if one could not eliminate silicon dioxide from the equation of Nagata, the appellant's independent claims do not exclude silicon dioxide from being the second dielectric material. So, the first dielectric material would become T_{x1}/E_{x1} and the second dielectric material would be noted as T_{SiO_2}/E_{SiO_2} . Basically, the appellant's equation is a simplified form of Nagata's equation, which is a

in the range of 25-70 nm or the specific materials (HfO₂, BaO, La₂O₃, Y₂O₃, and ZrO₂) of the first dielectric material. The examiner believes that the cited references show all of the elements of the claims and proper motivation for combining.

(1) In re the arguments that Nagata does not disclose the relationship $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$ (eq. 4 cited in appellant's brief and cited in claims 8 and 15), the examiner believes that Nagata shows this element of the claims in question. Nagata's initial formula (col. 4, lines 39-44) is used for finding the effective oxide thickness of a multi-layer stack of dielectrics including oxide. The variables of Nagata's formula are the same as variables of the appellant's formula. For instance:

Appellant's Variable	Nagata's Variable	Description
t_{ox}	T_{eff}	Thickness for a single gate dielectric of silicon dioxide
	T_{SiO_2}	Thickness of silicon dioxide (Nagata only)
k_{ox}	E_{SiO_2}	Dielectric constant of silicon dioxide
t_1, t_2	$T_{x1}, T_{x2}, T_{xn}, \text{etc.}$	Thickness of first, second, third, etc. other dielectric layers
k_1, k_2	$E_{x1}, E_{x2}, E_{xn}, \text{etc.}$	Dielectric constant of first, second, third, etc. dielectric layers

Nagata's formula starts off as:

$$T_{eff} = \left(\frac{T_{SiO_2}}{E_{SiO_2}} + \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} + \dots + \frac{T_{xi}}{E_{xi}} + \dots + \frac{T_{xn}}{E_{xn}} \right) E_{SiO_2}$$

Then the following operation is performed to solve for T_{eff} / E_{SiO_2} :

$$\frac{T_{eff}}{E_{SiO_2}} = \left(\frac{T_{SiO_2}}{E_{SiO_2}} + \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} + \dots + \frac{T_{xi}}{E_{xi}} + \dots + \frac{T_{xn}}{E_{xn}} \right)$$

standard way of finding the equivalent dielectric thickness of a multi-layered dielectric stack. The formula is used to calculate the equivalent effective thickness of silicon oxide or can be applied to other materials, thus the first and second dielectric materials are scalable for a set of feature size technologies as stated in the claims. Nagata therefore shows these elements of the claims.

The appellant additionally argues that Nagata does not teach a transistor having the first dielectric and the second dielectric, but teaches two transistors separated and electrically isolated from each other by a plurality of layers including a first layer and a second layer. As stated in the rejection above, Nagata shows in figures 21-25 that the transistor (shown completed in fig. 25) has a gate electrode (96) overlying a gate dielectric, the gate dielectric having a first material layer (82) of SiO_2 and a second material layer (84) of Al_2O_3 . That device is a MISFET and has the structure of a gate formed on the multi-layered dielectric. Therefore, Nagata also shows these elements of the claims.

(2) In re the rest of the appellant's arguments, the examiner believes that the combined references show the remaining elements of the claims. As stated in the rejection above, Momose was cited to cure the deficiencies of Nagata by teaching a device having a gate length in the range of 25-70 nm. It would have been obvious to one of ordinary skill in the art to make the gate length within the desired range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re*

Aller, 105 USPQ 233. However, as stated in the rejection, Momose clearly discloses a device having a dual layered gated dielectric and the gate length of the gate electrode being within the desired range. One of ordinary skill in the art would look to Momose to form a high performance semiconductor device having low power consumption (col. 16, 28-48 and col. 16, line 66-col. 17, line 32), improved current drive capability (col. 15, lines 13-31), and improved hot carrier reliability (col. 2, lines 52-58). Furthermore, the thickness of the gate dielectric is less than one-third the length of the gate since Momose teaches (col. 2, lines 52-58) as an example that the gate length may be 0.3 micrometers (300nm) and the insulating film thickness is less than 2.5 nm. One third of the gate length is 100 nm and obviously, the insulating thickness of 2.5 nm is less than 1/3 the gate length. The result is that hot carrier problems are reduced. No matter what the length of the gate, Momose has found that keeping the gate dielectric thin (around 2.5 nm) provides various benefits such as increased current drive capability (col. 15, lines 10-31). Therefore, Momose cures those deficiencies Nagata and shows proper motivation for the combination.

As stated in the rejection above, Moon was cited to cure the deficiencies of Nagata and Momose by teaching the specified dielectric materials of HfO_2 , BaO , La_2O_3 , Y_2O_3 , or ZrO_2 for the first dielectric material. Moon teaches that Y_2O_3 as a first dielectric and PZT as a second dielectric forms a good-quality ferroelectric material for a semiconductor device (col. 4, lines 1-12). Since the appellant lists Y_2O_3 as the first dielectric (claims 8 and 15) and PZT (claims 13 and 20) as the second dielectric, Moon is particularly relevant. Moon discloses that the materials and structure of the instant

Art Unit: 2815

invention are not novel and has known benefits. Therefore, Moon cures that deficiency of Nagata and Momose and shows proper motivation for the combination.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

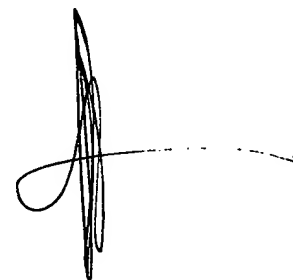
MEW

MEW

Conferees:

Tom Thomas, SPE of Art Unit 2815

T. T.

A handwritten signature in black ink, consisting of a large, stylized 'K' followed by a horizontal line extending to the right.

**KENNETH PARKER
SUPERVISORY PATENT EXAMINER**

AHH

Andrew Hirshfeld, SPE of Art Unit 2854